LISTING OF CLAIMS

1. (Previously Presented) A process for fabricating an electronic integrated circuit comprising:

a) forming, on a substrate of the circuit, of which a part is composed of absorbing material, a portion made of a sacrificial material coming into contact with one face of the part of the substrate composed of absorbing material;

b) forming a rigid portion in fixed contact with the substrate, on one side of the portion of sacrificial material opposite to said face of the part of the substrate composed of absorbing material; and

c) heating the circuit in order to create a volume substantially empty of material by absorption of the sacrificial material into the part of the substrate composed of absorbing material,

wherein the sacrificial material has a melting point in excess of 900°C and wherein the sacrificial material is chosen so as not to cause any material alteration of parts of the circuit in contact with the portion of sacrificial material prior to c) heating.

2. (Previously Presented) The process according to Claim 1, wherein the sacrificial material includes cobalt, nickel, titanium, tantalum, tungsten, molybdenum, silver, gold, iron and/or chromium.

3. (Previously Presented) The process according to Claim 1, wherein the absorbing material includes silicon, germanium, phosphorus, arsenic and/or antimony.

4. (Previously Presented) The process according to Claim 1, wherein the portion of sacrificial material is formed in a cavity below the level of a surface of the substrate.

5. (Previously Presented) The process according to Claim 1, wherein, at c) heating, the absorption of the sacrificial material into the part of the substrate composed of absorbing material results from a chemical reaction between the sacrificial material and the absorbing material.

6. (Previously Presented) The process according to Claim 1, wherein said volume substantially empty of material has a large cross section substantially parallel to a surface of the substrate.

7. (Previously Presented) The process according to Claim 1, further comprising, between a) forming and b) forming, forming of an intermediate layer, said intermediate layer being located, when b) forming is complete, between the portion of sacrificial material and the rigid portion.

8. (Previously Presented) The process according to Claim 1, wherein the volume substantially empty of material is situated between two electrodes of a capacitor belonging to said circuit.

9. (Previously Presented) The process according to Claim 8, wherein the rigid portion comprises a first electrode of the capacitor.

10. (Previously Presented) The process according to Claim 8, wherein the part of the substrate composed of absorbing material, after absorbing the sacrificial material in c) heating, comprises a second electrode of the capacitor.

11. (Previously Presented) The process according to Claim 8, wherein at least one of the two electrodes has a main surface substantially parallel to a substrate surface.

12. (Previously Presented) An electronic integrated circuit fabricated in accordance with the process of Claim 1.

13. (Withdrawn) The electronic integrated circuit according to Claim 12, wherein the volume substantially empty of material is located within a layer of metallization level of said circuit.

14. (Previously Presented) A process for forming an integrated circuit, comprising:

forming in an absorbing material layer a cavity;

depositing a sacrificial layer in the cavity, the sacrificial layer having a melting point in excess of a temperature used for circuit component fabrication heating;

filling the cavity with a fill material; and

heating the integrated circuit to a temperature sufficient to cause the sacrificial layer to be absorbed into the absorbing material layer and leave a void between the absorbing material layer and the fill material.

15. (Previously Presented) The process of claim 14 wherein the absorbing material layer is a semiconductor substrate layer.

16. (Withdrawn) The process of claim 14 wherein the absorbing material layer is a layer above a semiconductor substrate layer.

17. (Previously Presented) The process of claim 14 wherein circuit component fabrication heating comprises integrated circuit heat densification.

18. (Previously Presented) The process of claim 14 wherein heating comprises using the heating step to not only cause the sacrificial layer to be absorbed but also to drive silicidation of the integrated circuit.

19. (Previously Presented) The process of claim 14, wherein the sacrificial layer includes a material selected from the group consisting of cobalt, nickel, titanium, tantalum, tungsten, molybdenum, silver, gold, iron and chromium.

20. (Previously Presented) The process of claim 14, wherein the absorbing material layer includes a material selected from the group consisting of silicon, germanium, phosphorus, arsenic and antimony.

21. (Previously Presented) The process of claim 14 wherein the fill layer comprises an intermediate layer and an electrically conducting layer.

22. (Previously Presented) An integrated circuit, comprising:

an absorbing material layer into which a cavity has been formed; and

a fill layer that nearly fills the cavity, a void being provided between the fill layer and a bottom of the cavity,

wherein the absorbing material layer at the bottom of cavity includes an absorbed region where it has absorbed a sacrificed sacrificial layer whose absence creates the void.

23. (Previously Presented) The circuit of claim 22 wherein the absorbing material layer is a semiconductor substrate layer.

24. (Withdrawn) The circuit of claim 22 wherein the absorbing material layer is a layer above a semiconductor substrate layer.

25. (Previously Presented) The circuit of claim 22 wherein the absorbed sacrificial layer includes a material selected from the group consisting of cobalt, nickel, titanium, tantalum, tungsten, molybdenum, silver, gold, iron and chromium.

26. (Previously Presented) The circuit of claim 22, wherein the absorbing material layer includes a material selected from a group consisting of silicon, germanium, phosphorus, arsenic and antimony.

27. (Previously Presented) The circuit of claim 22 wherein the fill layer comprises an intermediate layer and an electrically conducting layer.

28. (Previously Presented) The circuit of claim 22 wherein the absorbed sacrificial layer has a melting point in excess of 900°C.

29. (Previously Presented) The circuit of claim 22 wherein the absorbed sacrificial layer has a melting point in excess of a temperature used for circuit component fabrication heating.

30. (Previously Presented) The circuit of claim 29 wherein circuit component fabrication heating comprises integrated circuit heat densification.

31. (Previously Presented) The circuit of claim 22 herein the absorbed sacrificial layer is absorbed into the absorbing material layer at the bottom of cavity during silicidation of the integrated circuit.

32. (Previously Presented) The circuit of claim 22 wherein the fill layer, void and absorbing material layer define a MIM-type integrated circuit capacitor structure.